12-14-99

A

DOCKET NO. : BERG-2462/C2346 **PATENT**

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In Re Application of:

Donald K. Harper, Jr.

Serial No.: Not yet assigned **Group Art Unit:** Not yet assigned

Filing Date: Herewith **Examiner:** Not yet assigned

For: ELECTRICAL CONNECTOR HOUSING

EXPRESS MAIL LABEL NO: EL531775146US
DATE OF DEPOSIT: December 13, 1999

Box ☒ Patent Application

☐ Provisional ☐ Design

Assistant Commissioner for Patents
Washington DC 20231

Sir:

PATENT APPLICATION TRANSMITTAL LETTER

Transmitted herewith for filing, please find

☒ A Utility Patent Application under 37 C.F.R. 1.53(b).

It is a continuing application, as follows:

☐ continuation ☐ divisional ☐ continuation-in-part of prior application number ___/_____.

☐ A Provisional Patent Application under 37 C.F.R. 1.53(c).

☐ A Design Patent Application (submitted in duplicate).

Including the following:

☐ Provisional Application Cover Sheet.

☒ New or Revised Specification, including pages 1 to 10 containing:

☒ Specification

☒ Claims

☒ Abstract

☐ Substitute Specification, including Claims and Abstract.

☐ The present application is a continuation application of Application No. _____ filed _____. The present application includes the Specification of the parent application which has been revised in accordance with the amendments filed in the parent application. Since none of those amendments incorporate new matter into the parent application, the present revised Specification also does not include new matter.

☐ The present application is a continuation application of Application No. _____ filed _____, which in turn is a continuation-in-part of Application No. _____ filed _____. The present application includes the Specification of the parent application which has been revised in accordance with the amendments filed in the parent application. Although the amendments in the parent C-I-P application may have incorporated new matter, since those are the only revisions included in the present application, the present application includes no new matter in relation to the parent application.

☐ A copy of earlier application Serial No. _____ Filed _____, including Specification, Claims and Abstract (pages 1 - @@), to which no new matter has been added TOGETHER WITH a copy of the executed oath or declaration for such earlier application and all drawings and appendices. Such earlier application is hereby incorporated into the present application by reference.

☐ Please enter the following amendment to the Specification under the Cross-Reference to Related Applications section (or create such a section) : "This Application: ☐ is a continuation of ☐ is a divisional of ☐ claims benefit of U.S. provisional Application Serial No. _____filed _____
_____

_____

_____.

☐ Signed Statement attached deleting inventor(s) named in the prior application.

☐ A Preliminary Amendment.

☒ Four (4) Sheets of ☒ Formal ☐ Informal Drawings.

☐ Petition to Accept Photographic Drawings.

☐ Petition Fee

☒ An ☒ Executed ☐ Unexecuted Declaration or Oath and Power of Attorney.

☒ An Associate Power of Attorney.

☐ An ☐ Executed ☐ Copy of Executed Assignment of the Invention to _____

_____.

☐ A Recordation Form Cover Sheet.

☐ Recordation Fee - $40.00.

☐ The prior application is assigned of record to _____

☐ Priority is claimed under 35 U.S.C. § 119 of Patent Application No. _____ filed _____ in _____ (country).

☐ A Certified Copy of each of the above applications for which priority is claimed:

☐ is enclosed.

☐ has been filed in prior application Serial No. _____ filed _____.

☐ An ☐ Executed or ☐ Copy of Executed Earlier Statement Claiming Small Entity Status under 37 C.F.R. 1.9 and 1.27

☐ is enclosed.

☐ has been filed in prior application Serial No. _____ filed _____, said status is still proper and desired in present case.

☐ Diskette Containing DNA/Amino Acid Sequence Information.

☐ Statement to Support Submission of DNA/Amino Acid Sequence Information.

☐ The computer readable form in this application _____, is identical with that filed in Application Serial Number _____, filed _____. In accordance with 37 CFR 1.821(e), please use the ☐ first-filed, ☐ last-filed or ☐ only computer readable form filed in that application as the computer readable form for the instant application. It is understood that the Patent and Trademark Office will make the necessary change in application number and filing date for the computer readable form that will be used for the instant application. A paper copy of the Sequence Listing is ☐ included in the originally-filed specification of the instant application, ☐ included in a separately filed preliminary amendment for incorporation into the specification.

☐ Information Disclosure Statement.

- ☐ Attached Form 1449.
- ☐ Copies of each of the references listed on the attached Form PTO-1449 are enclosed herewith.

☐ A copy of Petition for Extension of Time as filed in the prior case.

☐ Appended Material as follows: _____.

☒ Return Receipt Postcard (should be specifically itemized).

☐ Other as follows: _____

_____

_____.

FEE CALCULATION:

☐ Cancel in this application original claims _____ of the prior application before calculating the filing fee. (At least one original independent claim must be retained for filing purposes.)

			SMALL ENTITY		NOT SMALL ENTITY	
			RATE	FEE	RATE	FEE
PROVISIONAL APPLICATION			$75.00	$	$150.00	$
DESIGN APPLICATION			$155.00	$	$310.00	$
UTILITY APPLICATIONS BASE FEE			$380.00	$	$760.00	$760.00
UTILITY APPLICATION; ALL CLAIMS CALCULATED AFTER ENTRY OF ALL AMENDMENTS						
	No. Filed	No. Extra				
TOTAL CLAIMS	15 - 20 =	0	$9 each	$	$18 each	$ 0
INDEP. CLAIMS	3 - 3 =	0	$39 each	$	$78 each	$ 0
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM			$130	$	$260	$ 0
ADDITIONAL FILING FEE				$		$ 0
TOTAL FILING FEE DUE				$		$760.00

☒ A Check is enclosed in the amount of $ 760.00 .

☒ The Commissioner is authorized to charge payment of the following fees and to refund any overpayment associated with this communication or during the pendency of this application to deposit account 23-3050. This sheet is provided in duplicate.

☐ The foregoing amount due.

☒ Any additional filing fees required, including fees for the presentation of extra claims under 37 C.F.R. 1.16.

☒ Any additional patent application processing fees under 37 C.F.R. 1.17 or 1.20(d).

☐ The issue fee set in 37 C.F.R. 1.18 at the mailing of the Notice of Allowance.

☒ The Commissioner is hereby requested to grant an extension of time for the appropriate length of time, should one be necessary, in connection with this filing or any future filing submitted to the U.S. Patent and Trademark Office in the above-

identified application during the pendency of this application. The Commissioner is further authorized to charge any fees related to any such extension of time to deposit account 23-3050. This sheet is provided in duplicate.

SHOULD ANY DEFICIENCIES APPEAR with respect to this application, including deficiencies in payment of fees, missing parts of the application or otherwise, the United States Patent and Trademark Office is respectfully requested to promptly notify the undersigned.

Date: **December 13, 1999**

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ELECTRICAL CONNECTOR HOUSING

FIELD OF THE INVENTION

The present invention relates in general to an electrical connector and, more particularly, to a ball grid array (BGA) connector having a housing that can accommodate thermal cycling and circuit substrate or circuit board deformation or warpage characteristics.

BACKGROUND OF THE INVENTION

The drive to reduce the size of electronic equipment, particularly personal portable devices, and to add additional functions to such equipment, has resulted in an ongoing drive for miniaturization of all components, especially electrical connectors. Efforts to miniaturize connectors have included reducing the pitch between terminals in single or double row linear connectors, so that a relatively high number of I/O or other lines can be interconnected by connectors that fit within tightly circumscribed areas on the circuit substrates allotted for receiving connectors.

The drive for miniaturization has also been accompanied by a shift in preference to surface mount techniques (SMT) for mounting components on circuit boards. The confluence of the increasing use of SMT and the required fine pitch of linear connectors has resulted in approaching the limits of SMT for high volume, low cost operations. Reducing the pitch of the terminals increases the risk of bridging adjacent solder pads or terminals during reflow of solder paste. To satisfy the need for increased I/O density, array connectors have been proposed. Such connectors have a two dimensional array of terminals

mounted on an insulative substrate and can provide increased density. However, these connectors present certain difficulties with respect to attachment to the circuit substrate by SMT techniques because the surface mount tails of most, if not all, of the terminals must be beneath the connector body. As a result, the mounting techniques used must be highly reliable because it is difficult to visually inspect the solder connections to repair them if faulty.

In the mounting of an integrated circuit (IC) on a plastic or ceramic substrate, the use of a ball grid array (BGA) and other similar packages has become common. In a BGA package, spherical solder balls attached to the IC package are positioned on electrical contact pads of a circuit substrate to which a layer of solder paste has been applied, typically by use of a screen or mask. The unit is then heated to a temperature at which the solder paste and at least a portion or all of the solder ball melt and fuse to an underlying conductive pad formed on the circuit substrate. The IC is thereby connected to the substrate without need of external leads on the IC.

While the use of BGA and similar systems in connecting an IC to a substrate has many advantages, a corresponding means for mounting an electrical connector or similar component on a printed wiring board (PWB) or other substrate has yet to be developed. It is important for most situations that the substrate-engaging surfaces of the solder balls are coplanar to form a substantially flat mounting interface, so that in the final application the balls will reflow and solder evenly to a planar printed circuit board substrate. Any significant differences in solder coplanarity on a given substrate can cause poor soldering performance when the connector is reflowed onto a printed circuit board.

Another problem presented in soldering connectors to a substrate is that connectors often have insulative housings that have relatively complex shapes, for example, ones having numerous cavities. Residual stresses in such housings can result from the molding process, from the buildup of stress as a result of contact insertion, or a combination of both. These housings may become warped or twisted either initially or upon heating to temperatures necessary in SMT processes, such as temperatures necessary to reflow the solder balls. Such warping or twisting of the housing can cause a mismatch between the connector assembly and the PWB, resulting in unreliable soldering because the surface mounting elements, such as solder balls, are not sufficiently in contact with the solder paste or close to the PWB prior to soldering.

One drawback of BGA packages is that the coefficient of thermal expansion (CTE) of the material used in the connector housing is very different from the CTE of the PWB. The different CTEs affects the performance and reliability of the electrical connections by causing stress on solder joints and wire bonds, thereby leading to deformation and warpage of the PWBs or IC chips and chip carriers that are to be connected to the package. The greater the differential displacements created by CTE mismatch during thermal changes, the greater concern for the electrical integrity of the system.

BGA packages are subjected to high temperatures during processing, testing and soldering. Accordingly, it is important that the package be able to withstand high temperature variations without inhibiting or degrading a reliable electrical connection. A need, therefore, exists for reliably and efficiently mounting high density electrical connectors on substrates by surface mounting techniques.

SUMMARY OF THE INVENTION

The present invention is directed to a connector for reducing the effects of the differential in the coefficient of thermal expansion of the connectors and the underlying circuit board. The connector in accordance with the present invention can be mounted on a known circuit board or the like and could receive an electrical component or a mating connector. The present invention preferably uses ball grid array (BGA) surface mount technology.

Electrical connectors according to the present invention provide high I/O density and reliable attachment to circuit substrates by SMT techniques. These connectors exhibit high coplanarity along the mounting interface. Coplanarity of the surface mounting interface of the connector is maintained by providing an insulative connector housing in which stress buildup is avoided. The present invention accommodates the deformation or warpage caused by thermal cycling that would otherwise cause the stress buildup. The connector avoids stress buildup by providing a connector housing that incorporates compliant sections corresponding to the areas where the greatest deformation in the connector is expected. According to this aspect of the invention, the housing has notches or slots at locations furthest from the neutral point (NP) of the connector (i.e., around the corners). By means of this arrangement, stress buildup is avoided, so as to minimize warping and twisting of the housing.

Electrical connectors of the present invention are ones in which one or more

terminals are connectable by a fusible electrically conductive material to a substrate. This fusible electrically conductive material is a solder mass, preferably comprising a solder ball that can be reflowed to provide the primary electrical current path between the terminal and a circuit substrate.

The foregoing and other aspects of the present invention will become apparent from the following detailed description of the invention when considered in conjunction with the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a top perspective view of the conventional BGA interface connector;

Fig. 2 is a bottom perspective view of the BGA interface connector of Fig. 1;

Fig. 3 is a side view of an exemplary BGA interface connector in accordance with the present invention;

Fig. 4 is a perspective view of the BGA interface connector of Fig. 3; and

Fig. 5 is a bottom perspective view of the BGA interface connector of Fig. 3.

DESCRIPTION OF EXEMPLARY EMBODIMENTS AND BEST MODE

Generally, the present invention provides an electrical connector preferably surface mounted to a circuit substrate using, as one example, ball grid array (BGA) technology. In accordance with the present invention, the housing of the connector has slots or other shaped features at selected locations on the housing to prevent warpage when mounted or laminated to a substrate such as a PWB, PCB, or semiconductor chip.

A perspective view of a conventional interface connector, such as a BGA connector, is shown in Fig. 1. Fig. 2 is a bottom perspective view of the exemplary interface connector. The BGA package 10 comprises a housing 15 made from a suitable dielectric material. A plurality of contacts 11 extend through the housing with one end adjacent a lower surface of the substrate. The contacts comprise an electrically conductive material such as a copper alloy. A fusible element 35, such as a solder ball, is fused to a surface of the contact and at least partially within an aperture 40 on the bottom of housing 15. Conductive solder balls 35 are metallurgically wetted to contacts during a reflow process. More particularly, flux is applied to the contacts and/or the aperture 40. The spherical solder balls 35 are then placed

in the paste temporarily. The assembly is then inserted into a reflow furnace (not shown) and heated. This causes the balls 35 and solder paste to wet and melt onto the surfaces of their respective contacts and to assume a generally spherical shape. Conductive solder balls 35 are spaced a pitch apart, which can be on the order of 1.0 to 1.8 mm. International Publication number WO 98/15989 (International Application number PCT/US97/18056), herein incorporated by reference, describes in further detail the methods of securing a solder ball to a contact and/or a circuit substrate. The contacts form a series of rows and columns on the housing of the connector. The solder balls, when fused to the contacts, preferably all have the same elevation. This ensures a proper connection to an underlying printed wiring board (PWB).

Any balls formed of solder that flows completely, i.e., melts completely and then resolidifies, or that even partially reflows, can be used. Examples are tin bismuths, 63-37 eutectic, and other newer solders which reflow at temperatures in the range of 183° C. The solder reflow processes used herein generally heat the solder balls 35 up to 225° C to 240° C.

The conductive solder balls 35 are connected to an underlying assembly or PWB using either the same solder reflow process that fuses the solder balls 35 to the contacts, or a subsequent reflow step. The PWB has a plurality of contact pads arranged in a pattern. Conductive solder balls 35 connect to the contact pads to form solder joints. After the mounting process, solder joints take a flattened spherical shape defined by solder volume and wetting areas. The number and arrangement of conductive solder balls 35 on the lower surface of substrate depends on circuit requirements including input/output (I/O), power and ground connections.

More particularly, the BGA assembly 10 is connected to a previously-manufactured circuit board which has an array of conductive pads on it. Solder paste is screened (using a stencil and squeegee) onto the circuit board pads. A placement machine (not shown) places the assembly 10 onto the tops of the solder paste, and the resulting construction is heated in a reflow furnace (also not shown). The balls 35 then reflow onto the circuit board pads.

The housing comprises a plurality of passageways 25 into which the contacts can be inserted. The passageways 25 preferably frictionally retain the contacts in the housing

until reflow. In this manner, the contacts will be electrically connected to the underlying PWB that the BGA package is ultimately connected to using the BGA mounting technology. Thus, the connector provides, for example, a board-to-board interconnection.

The connector 10 could have a wall disposed around the periphery of the connector to help guide a mating connector (not shown). The wall can include suitable keying features (not shown) to ensure proper mating with the mating component.

The difference in the coefficient of thermal expansion (CTE) of the substrates, such as the PWBs, and the connector 10, and the coplanarity of the fusible elements 35 are two important considerations with large scale array connectors. CTE differential can introduce stress into the solder joints that couple the connector 10 and the PWB or substrate. Solder joint stress potentially reduces the thermal reliability of the connector 10. CTE differential can also warp the connector 10. Connector warp potentially misaligns the mating connectors, which increases the required peak insertion force. Connector warp may also affect the coplanarity of the fusible elements 35 that couple the connector to the substrate.

In accordance with the present invention, locations at the greatest distance from the neutral point (NP) of the connector are conditioned to allow the areas to flex so as to absorb stresses that could damage the solder joint. In other words, the housing is not as strong and bends easier. This reduces solder joint stress, thereby accommodating warp. Typically, the corners of housing 15 comprise the greatest distance to neutral point (DNP). The conditioning can involve notching areas of the housing.

Fig. 3 is a side view of an exemplary BGA interface connector in accordance with the present invention, Fig. 4 is a perspective view of the BGA interface connector of Fig. 3, and Fig. 5 is a bottom perspective view of the BGA interface connector of Fig. 3. The housing 15 has openings 12 in sidewalls that are placed at desired locations so as to allow the housing 15 to be compliant along desired axes (typically perpendicular to the plane of the circuit substrate). As a result, a reduction in solder joint stress between the connector 10 and its mounting substrate (such as an underlying PWB) results. Thus, during thermal cycling, the effects of the differential in the coefficient of thermal expansion of the PWB substrate and the connector 10 are minimized. Moreover, the coplanarity of the contacts is improved. Since the areas of housing 15 near openings 12 tend to flex, preferably no contacts are placed in housing 15 adjacent these locations.

It should be noted that the disruption in the material in the frame of the housing 15 can be any shape, and positioned anywhere on the frame, in order to give the desired effects.

The present invention addresses the effects of CTE mismatch by providing slots or notches in the connector housing. Thus, the present invention solves a reliability failure mechanism, CTE mismatch.

Although the present invention has been described with respect to BGAs, other packages, such as μBGA and other chip scale grid array (CSGA) type packages, flip chip, and C4 type connections can also be used with the present invention.

Although illustrated and described herein with reference to certain specific embodiments, the present invention is nevertheless not intended to be limited to the details shown. Rather, various modifications may be made in the details within the scope and range of equivalents of the claims and without departing from the invention.

What is claimed:

1. An electrical connector, comprising:

a housing;

a plurality of surface mount contacts; and

areas of reduced rigidity in the housing.

2. The electrical connector according to claim 1, wherein the areas of reduced rigidity in the housing are located at positions furthest from a neutral point of the connector.

3. The electrical connector according to claim 1, wherein each of the areas of reduced rigidity comprises one of a notch and a slot.

4. The electrical connector according to claim 1, wherein the areas of reduced rigidity are disposed to absorb stress and accommodate warp.

5. The electrical connector according to claim 1, wherein the housing comprises a dielectric material.

6. The electrical connector according to claim 1, wherein the surface mount contacts comprise solder balls.

7. The electrical connector according to claim 6, wherein the surface mount contacts comprise ball grid array surface mount contacts.

8. A housing for an electrical connector, comprising:

a frame; and

areas of reduced rigidity in the frame.

9. The housing according to claim 8, wherein the areas of reduced rigidity are located at positions furthest from a neutral point of the connector.

10. The housing according to claim 8, wherein each of the areas of reduced rigidity comprises one of a notch and a slot.

11. The housing according to claim 8, wherein the areas of reduced rigidity are disposed to absorb stress and accommodate warp.

12. A method of reducing rigidity in a housing of an electrical connector, comprising:

determining a neutral point of the connector; and

removing a portion of the housing at a position relative to the neutral point.

13. The method according to claim 12, wherein the position is furthest from the neutral point.

14. The method according to claim 12, wherein the position is located to absorb stress and accommodate warp.

15. The method according to claim 12, wherein the portion is one of a slot and a notch.

ABSTRACT

A connector is provided for reducing the effects of differential coefficient of thermal expansion of the connector and the underlying circuit board. The connector exhibits high coplanarity along the mounting interface by providing an insulative connector housing in which stress buildup is avoided. The connector housing incorporates compliant sections corresponding to the areas where the greatest deformation in the substrate is expected. The housing has notches or slots at locations furthest from the neutral point (NP) of the connector (i.e., around the corners). By means of this arrangement, stress buildup is avoided, so as to minimize warping and twisting of the housing.

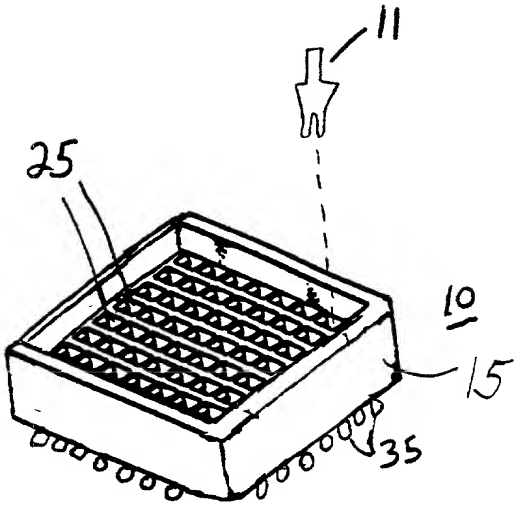

FIG. 1

PRIOR ART

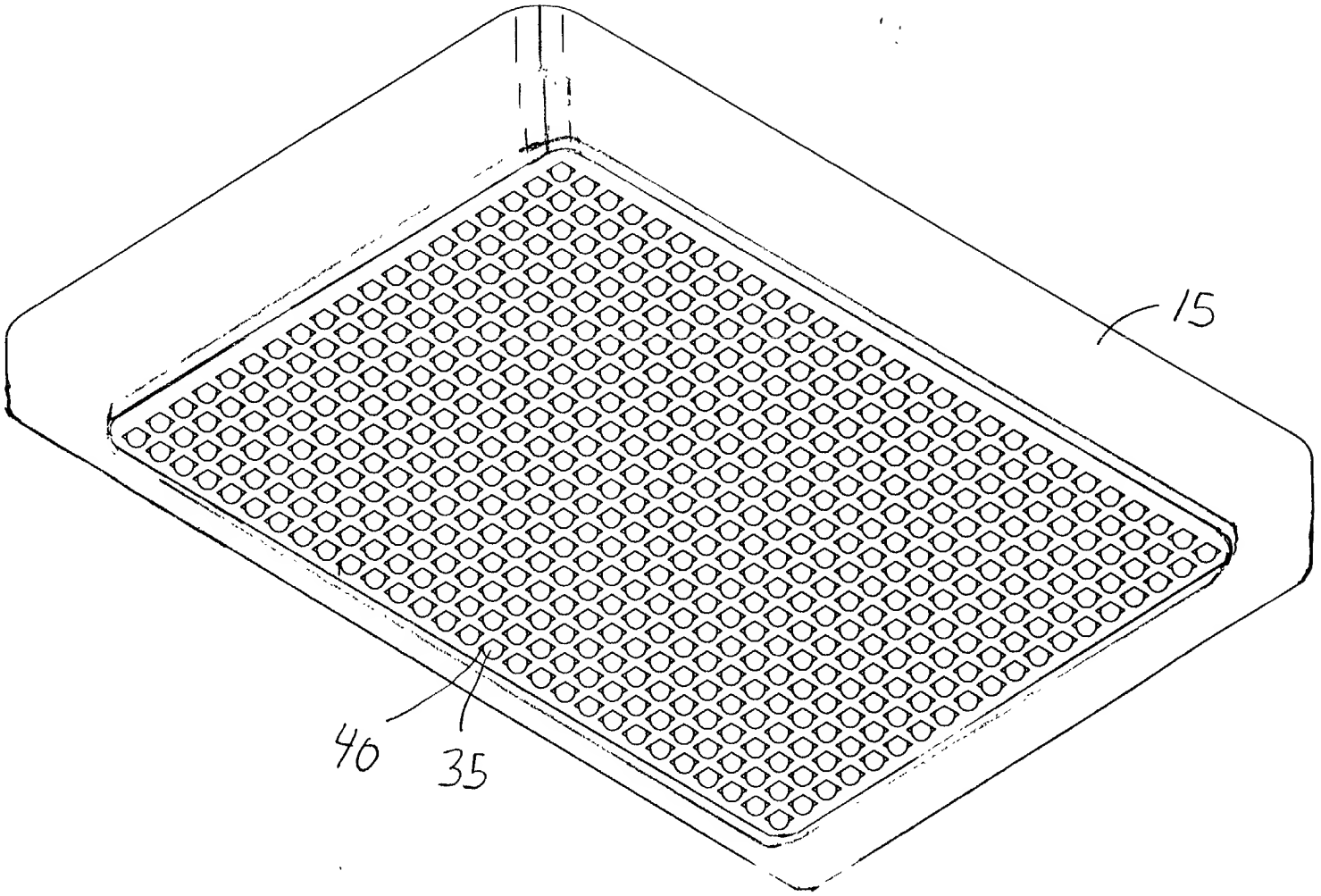

FIG. 2
PRIOR ART

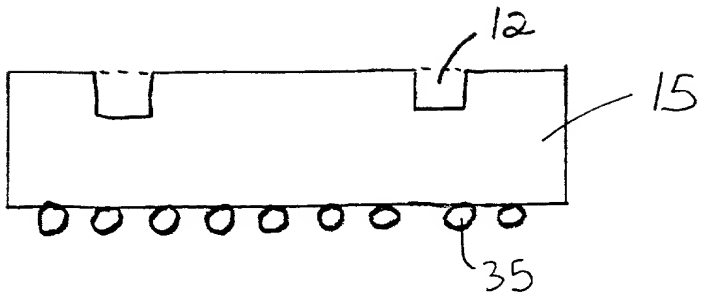

FIG. 3

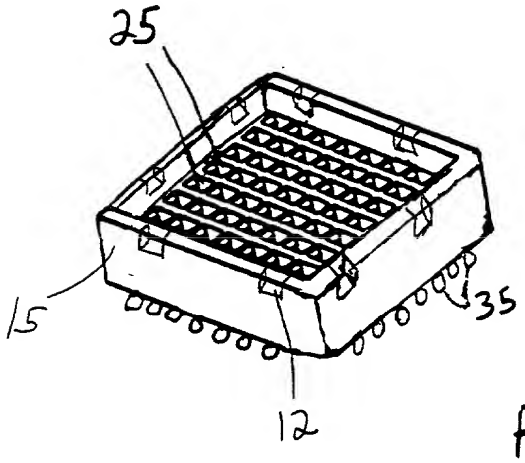

FIG. 4

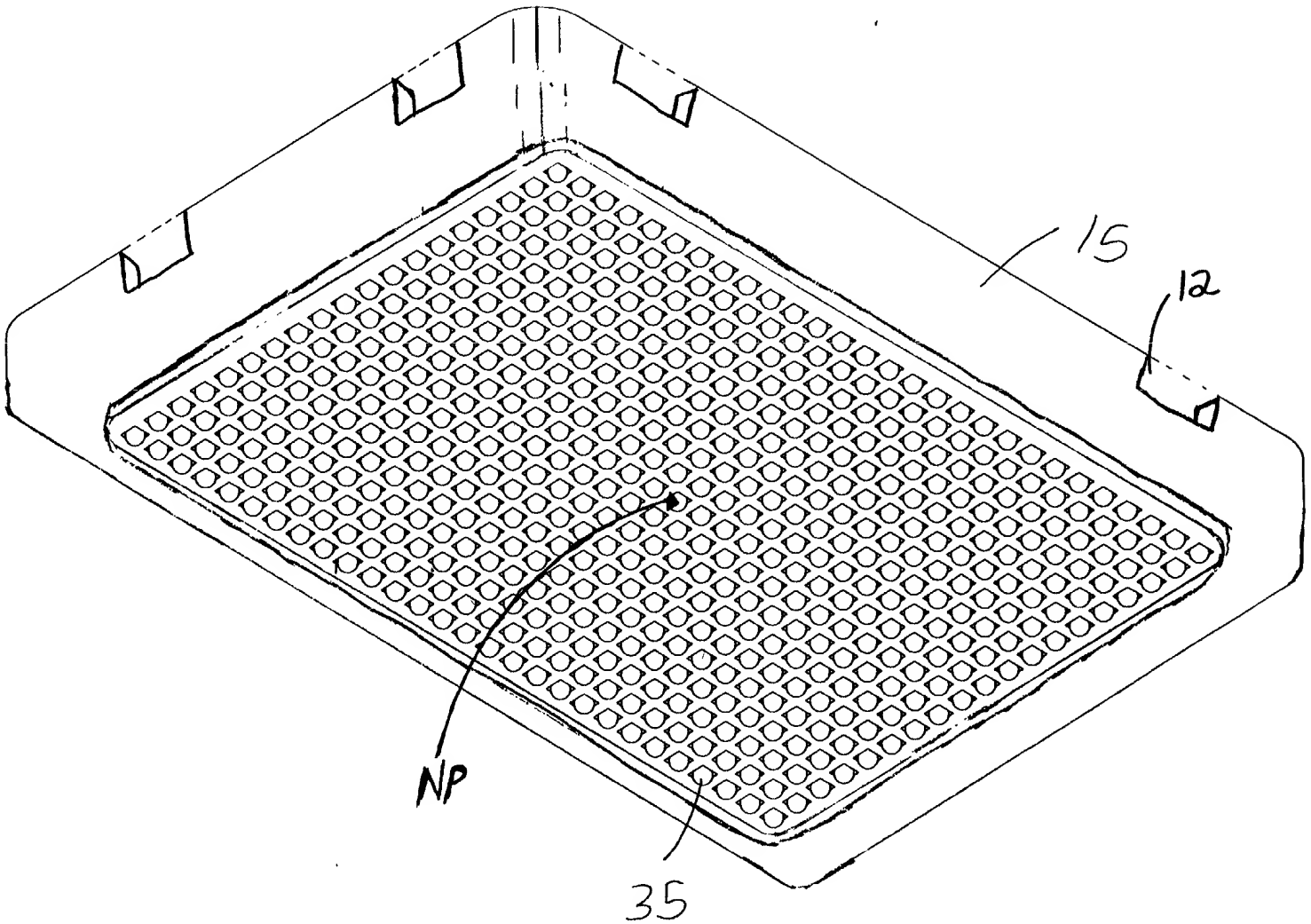

FIG. 5

DOCKET NO. BERG-2462/C2346 **PATENT**

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In Re Application of:

Donald K. Harper, Jr. **Group Art Unit:** Not yet assigned

Examiner: Not yet assigned

For: ELECTRICAL CONNECTOR HOUSING

DECLARATION AND POWER OF ATTORNEY

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name; and

I believe that I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a

☒ Utility Patent ☐ Design Patent

is sought on the invention, whose title appears above, the specification of which:

☒ is attached hereto.

☐ was filed on _____ as Serial No. _____ .

☐ said application having been amended on _____ .

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose to the U.S. Patent and Trademark Office all information known to be material to the patentability of this application in accordance with 37 CFR § 1.56.

I hereby claim foreign priority benefits under 35 U.S.C. § 119(a-d) of any **foreign application(s)** for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of

any application on which priority is claimed:

Priority Claimed (If X'd)	Country	Serial Number	Date Filed
☐			
☐			
☐			
☐			

I hereby claim the benefit under 35 U.S.C. § 120 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of 35 U.S.C. § 112, I acknowledge the duty to disclose to the U.S. Patent and Trademark Office all information known to be material to patentability as defined in 37 CFR § 1.56 which became available between the filing date of the prior application and the national or PCT international filing date of this application:

Serial Number	Date Filed	Patented/Pending/Abandoned

I hereby claim the benefit under 35 U.S.C. § 119(e) of any United States provisional application(s) listed below:

Serial Number	Date Filed

I hereby appoint the following persons as attorney(s) and/or agent(s) to prosecute this application and to transact all business in the Patent and Trademark Office connected therewith:

M. Richard Page, Esq.	Registration No. 25,299
Daniel J. Long, Esq.	Registration No. 29,404
Brian J. Hamilla, Esq.	Registration No. 38,482

of **FRAMATOME CONNECTORS INTERNATIONAL/BERG ELECTRONICS GROUP, INC.,** 825 Old Trail Road, Etters, Pennsylvania 17319 and

John P. Donohue, Jr., Esq.	Registration No. 29,916
Jonathan M. Waldman, Esq.	Registration No. 40,861

of **WOODCOCK WASHBURN KURTZ MACKIEWICZ & NORRIS LLP,** One Liberty Place - 46th Floor, Philadelphia, Pennsylvania 19103

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I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Name: Donald K. Harper, Jr.	
Mailing Address: 414 North 48th Street Harrisburg PA 17111	D. Harper **Signature** **Date of Signature:** 12-10-99 D. Harper
City/State of Actual Residence: Harrisburg PA 17111	**Citizenship:** United States of America

Name:	
Mailing Address:	_____ **Signature** **Date of Signature:** _____
City/State of Actual Residence:	**Citizenship:** _____

Name:	
Mailing Address:	_____ **Signature** **Date of Signature:** _____
City/State of Actual Residence:	**Citizenship:** _____

DOCKET NO. BERG-2462/C2346 **PATENT**

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Serial No.: Not yet assigned **Group Art Unit:** Not yet assigned

Filed: Herewith **Examiner:** Not yet assigned

For: ELECTRICAL CONNECTOR HOUSING

Assistant Commissioner for Patents
Washington DC 20231

Sir:

ASSOCIATE POWER OF ATTORNEY

The undersigned, of the firm WOODCOCK WASHBURN KURTZ MACKIEWICZ & NORRIS LLP, One Liberty Place - 46th Floor, Philadelphia, Pennsylvania 19103, Attorney and/or Agents for Applicant(s), hereby appoints the following:

Robert B. Washburn	Registration No. 16,574	Michael P. Straher	Registration No. 38,325
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John J. Mackiewicz	Registration No. 19,709	Anthony J. Rossi	Registration No. 24,053
Norman L. Norris	Registration No. 24,196	Michael J. Swope	Registration No. 38,041
Albert W. Preston, Jr.	Registration No. 25,366	Michael J. Bonella	Registration No. 41,628
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Henrik D. Parker	Registration No. 31,863	Maureen Gibbons	Registration No. 44,121
Suzanne E. Miller	Registration No. 32,279	Steven H. Meyer	Registration No. 37,189
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Mark DeLuca	Registration No. 33,229	Michael K. Jones	Registration No. 41,100
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Michael P. Dunnam	Registration No. 32,611	Hans J. Crosby	Registration No. 44,634
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his/her associates with full power to prosecute the above-identified application and to transact all business in the Patent Office connected therewith and requests that correspondence continue to be directed to the firm of WOODCOCK WASHBURN KURTZ MACKIEWICZ & NORRIS LLP at the above address.

Date: **December 13, 1999**

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